

REMARKS

Reconsideration of the application, as amended, is respectfully requested. By this amendment, claims 1, 9 and 15 have been amended, and new claims 24-28 have been added.

The amendments to claims 1, 9 and 15 define, the two processors (described earlier in these claims) using said parallel data highways at the high data rate interface and thereby communicating at a high data rate using said parallel data highways. Support for this limitation is found in the original specification, as found on page 4, line 18 - page 5, line 13.

In the Office Action, claims 21-23 were rejected under 35 U.S.C. §112, relating to antecedent basis for "the integrity" in claim 21. Claim 21 has been changed as suggested.

In the Office Action, claims 1-20 were rejected under 35 U.S.C. §103. Specifically, claims 1, 4, 5, 8, 9, 12, 13, 15, 18 and 19 were rejected over U.S. Patent No. 6,101,198 (Koenig, et al.). Claims 2, 3, 10 and 11 were rejected over Koenig, et al. taken in view of the admitted prior art and U.S. Patent No. 6,415,348 (Mergard et al.). Claims 6, 7 and 14 were rejected over Koenig, et al. and U.S. Patent No. 6,058,111 (Beyda, et al.). Claim 16 was rejected over Koenig, et al. and U.S. Patent No. 6,301,291 (Rouphael, et al.). Claim 17 was rejected over

Koenig et al. taken and U.S. Patent No. 5,063,592 (Cannella, et al.). These rejections, as applied to the amended claims, are respectfully traversed.

As previously indicated, the invention provides the advantage of two processors using parallel data highways outputting to a high data rate interface. In addition, the applicant describes two processors which use the parallel data highways at the high data rate interface and thereby communicate at the high data rate using the parallel data highways.

In contrast, Koenig, et al. shows a single field programmable gate array (FPGA) 34. The FPGA is depicted with separate MUX and de-MUX circuits, and each of the MUX and de-MUX representations is depicted as connected to a pair of T-1 lines through framers connected separately on the MUX and de-MUX sides. This appears to provide a frame relay function. The FPGA is connected to a single DSP 24 which in turn is connected to a host DSP functioning with a data port operating at 1.5 Mbps (a frame relay connection port). All of this is separate from the operation of the present invention, which uses the parallel data highways to transfer data to a wireless interface. This is in concept and function contradictory to Koenig's device for transferring data to through a single processor to multiple T-1 frame relay connections. Koenig, et al. mention a radio link but do not suggest using parallel data highways in association with a radio link.

Specifically, Applicants describe the use of an ISDN interface but separate from the wireless interface. See page 3, line 20 - page 4, line 3.

Referring to claim 1, applicant specifies:

- a wireless interface
- the wireless interface connected to a plurality of parallel data highways
- outputting data to the high data rate interface and the wireless interface
- each parallel data highway partially dedicated to a separate function
- a second processor sending data using a single one of the parallel data highways
- the two processors using said parallel data highways at the high data rate interface
- the processors communicating at a high data rate using said parallel data highways

Similar limitations appear in claims 9 and 15.

Looking at the cited section of the Applicant's prior art descriptions, the use of wireless modems is described. While a frame relay may be considered to be a type of modem, there is no suggestion anywhere in either the prior art descriptions or the cited references that dual processors be used to achieve a function performed

by a frame relay. There also is no suggestion in the prior art of record to use two processors for separate data highways. Accordingly, the combination would be inappropriate as a description of a wireless modem. Furthermore there is no suggestion that such a configuration include multiple data processors. Even if the use of a wireless modem can be associated with a T-1 frame relay connection, the use of multiple processors in combination with a wireless modem is neither shown nor suggested by any combination of the prior art of record.

Further, there is no prior art incentive to modify the prior art T-1 frame relay to accommodate the functions of the present invention. In a wireless system, there can be multiple types of connections within a single communications link, such as primary channel, high speed secondary channel, IEEE 802 or "hot spot" services, etc. There can also be a multiplicity of primary channels on a spread spectrum communications link. In contrast, the user of a frame relay of Koenig, et al. would apply the frame relay either to the T-1 lines or to unused T-1 bandwidth on the T-1 lines. There is no suggestion of applying such a system to wireless technology implemented with parallel data highways. Therefore Koenig, et al. "teaches away from" the present invention.

It is further noted that, as applied to each of independent claims 1, 9 and 15, the prior art citation of a single gate array describes communicating through two

T-1 lines, using a single set of multiplexing framers and a single set of demultiplexing framers. This does not suggest using two processors communicating through a wireless interface using parallel data highways.

With respect to claim 9, the use of the T-1 lines or the T-1 lines and their associated analog lines does not provide a suggestion of implementation of a wireless modem. To the contrary, the concept of a T-1 line is that of a fixed service connection which can be treated as providing the T-1 or frame relay function or treated as providing the associated analog bandwidth (eg., a 24T-1 line in its classical implementation). In contrast, Applicants' operation with a wireless connection provides an ability to use, for example, multiple wireless channels. This is different in nature from the T-1 frame relay described by Koenig, et al.

Regarding claims 4, 5, 12, 13 and 19, the prior art use of multiple data highways fails to suggest the present invention's claimed use of a wireless interface using separate processors communicating through multiple highways. Koenig, et al describe a single gate array communicating through two T-1 lines, using a single set of multiplexing framers and a single set of demultiplexing framers. This does not suggest using different processors communicating through a wireless interface using parallel data highways.

Regarding claim 15, Applicants respectfully disagree with the assertion that Koenig, et al. disclose a radio network terminal. To the contrary, Koenig, et al.

describe transmission "lines". While "lines" can be used to describe radio links, there is no such suggestion in Koenig, et al. To the contrary, Koenig, et al. describe T-1 lines, which are typically leased line connections capable of carrying data at 1,544,000 BPS. The rejection of claim 15 goes on to describe particular functions of frame relays, including the ability to send and receive data over the separate T-1 lines. Applying this, a combination of Koenig, et al. with the present invention would enable one to use Applicants' wireless modem interface in a frame relay apparatus. Such a combination would necessarily require Applicants' disclosure and is therefore a "hindsight application" of Applicants' invention.

Claims 2, 3, 10, 11 and 20 were rejected over Koenig, et al., or over Koenig, et al. and Mergard, et al. These rejections are respectfully traversed. While the use of an ION-2 interface or a PCM interface is described, there is no suggestion that a wireless link be used in association with parallel data highways. Accordingly, claims 2, 3, 10, 11 and 20 define patentable subject matter.

Claims 6, 7 and 14 were rejected over Koenig, et al. taken in view of Beyda, et al. This rejection is respectfully traversed. There is no suggestion in Beyda, et al that a plurality of port controllers be used in association with a wireless interface and parallel data highways operating through a wireless interface. Accordingly, claims 6, 7 and 14 define patentable subject matter.

Claim 16 was rejected over Koenig, et al. taken in view Roupael, et al. This rejection is respectfully traversed. There is no suggestion in this prior art combination that these references support the combination as per the elements claim 16.

Claim 17 was rejected over Koenig, et al. taken in view of U.S. Patent No. 5,063,592 (Cannella, et al.). These rejections, as applied to the amended claims, are respectfully traversed. As with the other references, there is no suggestion in Cannella, et al. that parallel data ports be combined with a high speed interface. Accordingly, claim 17 is patentable over the cited combination.

Claim 21 had been rejected over U.S. Patent 5,483,556 (Pillan, et al.), taken in view of U.S. Patent 5,381,422 (Shimizu). This rejection is respectfully traversed. Pillan, et al. describes compression at two levels, although in association with framing and storing of data, but fail to suggest the use of a wireless link. The terminology "data terminal" is used and cited at column 2, lines 61-65, but this fails to suggest wireless transmission. To the contrary, data terminal equipment (DTE) is generally considered to be a reference to a digital device sending or receiving data over data carrier equipment (DCE). This use of the terminology "data terminal" is not merely speculative, as evidenced by the use of similar DTE/DCE terminology at col. 3, line 65 - col. 4, line 2. Shimizu is cited as showing the use of error correction of data; however, there is no suggestion of the claimed use of a wireless interface.

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Therefore, the prior art of record, taken alone or in combination, fail to suggest an HDLC interface.

New claims 24-28 present the limitations of claim 21, applied to limit claims 1, 9 and 15. While it is Applicants' position that claims 1, 9 and 15 are novel over the cited art of record, it is further pointed out that there is no suggestion in the prior art of record to combine these claims (claims 1, 9 and 15) with the features of claim 21.

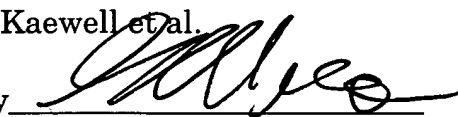
It is therefore submitted that the application, as presently amended, defines patentable subject matter. Therefore, the application is in a condition for allowance. Such allowance at an early date is respectfully requested.

If the Examiner feels that a conference will expedite the prosecution of this case, the Examiner is cordially invited to call the undersigned. To that end, an Examiner's amendment to this case would be welcomed and appreciated.

Respectfully submitted,

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